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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANIL SETH, RAVINDRA B. KESKAR, and R. VENUGOPAL

Appeal 2008-2929
Application 10/087,296
Technology Center 2100

Decided:[1] April 22, 2009

Before LEE E. BARRETT, JOSEPH L. DIXON, and
CAROLYN D. THOMAS, *Administrative Patent Judges.*

DIXON, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-44. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

A. INVENTION

The invention at issue on appeal relates to a technique for compiling computer code to reduce energy consumption while executing the code. (Spec. 1.)

B. ILLUSTRATIVE CLAIM

Claim 1, which further illustrates the invention, follows.

1. A method of compiling computer code including power-down instructions to reduce power consumption during execution of the code while satisfying user-specified real-time performance constraints on a microprocessor, comprising:

identifying one or more potential locations in the computer code where the power-down instructions can be inserted;

selecting locations to insert the power-down instructions from the identified potential locations in the code based on reducing power consumption and satisfying user-specified real-time performance constraints; and

inserting the power-down instructions in the selected locations to reduce the power consumption during the execution of the code while satisfying user-specified real-time performance constraints.

C. REFERENCES

The Examiner relies on the following references as evidence:

Bartley US 6,219,796 B1 Apr. 17, 2001

Y. Li and J. Henkel. *A Framework for Estimating and Minimizing Energy Dissipation of Embedded HW/SW Systems*, In Proceedings of the Design Automation Conference, pp. 188-193, (1998.) (Hereinafter Li)

G. Ramalingam, *Data Flow Frequency Analysis*, In Proceedings of the SIGPLAN '96 Conference on Programming Language Design and Implementation, pp. 267-277, (1996.) (Hereinafter Ramalingam)

D. REJECTIONS

The Examiner makes the following rejections.

Claims 1, 2, 11-15, 22-25, 32-36, 43, and 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bartley in view of Li.

Claims 3-10, 16-21, 26-31, and 37-42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bartley in view of Li and further in view of Ramalingam.

II. ISSUE

Have Appellants shown that the Examiner erred in the rejection based upon obviousness? Specifically, have Appellants shown that the prior art references of Bartley and Li do not teach or suggest satisfying user-specified real time performance constraints on the microprocessor as recited in independent claim 1 and have Appellants shown that the teachings of Bartley and Li are not properly combinable?

III. PRINCIPLES OF LAW

35 U.S.C. § 103(a)

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. *KSR*, 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. 1727, 1739 (2007)). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined

device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162 (citing *KSR*, 127 S. Ct. at 1740-41).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

IV. ANALYSIS

Appellants have two main contentions. First, Appellants contend the prior art references of Bartley and Li do not teach or suggest satisfying user-specified real time performance constraints on the microprocessor as recited in independent claim 1. Second, Appellants contend that the teachings of Bartley and Li are not properly combinable.

From our review of the Examiner's stated rejections, we find that the Examiner has set forth a sufficient initial showing of obviousness. Therefore, we look to Appellants' Briefs to show error in the Examiner's initial showing of obviousness.

With respect to the combination of the teachings of Bartley and Li, we find the Examiner's line of reasoning, as expressed in the Answer at pages 17-19, to amply support the Examiner's reliance on the teachings and suggestions within the Li reference. We find the Examiner's reliance Li evidences that the hardware modifications to optimize the hardware would have necessarily impacted upon the software. Therefore, skilled artisans would have appreciated that corresponding modifications to the software would also be needed. In combination with the teachings of the Bartley reference concerning the insertion of power-down instructions to turn off

functional units during program execution, additional power down instructions may additionally be required. Therefore, we find the Examiner's combination to be reasonable in light of the Examiner's explanation thereof. Additionally, we find the Examiner's explanations and reasoning in the responsive arguments at pages 16-29 to be reasonable in the Examiner's further explanation of how the prior art teachings teach and fairly suggest the claimed invention.

Appellants submit that neither reference discloses the use of power down instructions based upon user-specified real-time performance constraints. (App. Br. 9). We agree with Appellants since the Examiner has relied upon each of the two references for a portion of the argued limitation. However, Appellants' arguments directed to the individual teachings of the references with respect to the claim limitations is not persuasive of error in the Examiner's initial showing of obviousness because it is the combination of references that we must consider. Appellants submit that Li does not even relate to the use of power-down instructions, but rather relates to a very specific instance of hardware modifications and as such, Li is not properly combinable and with Bartley. (App. Br. 9-10). Appellants further contend that the presently claimed invention contributes to the art in that there are many places in code where a power down instruction could be added, and the claimed invention allows one to determine where to put those power down instructions to optimize power consumption within the user-specified constraints to make sure that the overall program performance is as desired. (App. Br. 10). We find Appellants' contention to be unpersuasive since Appellants' contention is not commensurate in scope with the express language recited in independent claim 1. Independent claim 1 sets forth

steps of "identifying...," "selecting...," and "inserting...." wherein there is no step of "determining" where to put the power down instructions and no step of "optimizing."

Appellants contend that the present invention allows a trade-off between performance and power conservation based upon user-specified constraints for execution of program code. (App. Br. 10).

Appellants contend that while Bartley determines functional units of a processor which will not be used during execution of a program wherein the functional units are shut down to conserve power, Bartley is only related to shut down for efficient power use and not for code performance. (App. Br. 10-11). We disagree with Appellants' interpretation of the teachings of Bartley and find that Bartley at column 7 suggests use of intermediate power down levels that are specifically useful to avoid delays in restoring power. In other words, after a full power down instruction a power up instruction or a non-power down instruction might result in the delay that would not occur if an intermediate power down instruction had been used. Clearly, Bartley is not solely concerned with power conservation and suggests and considers functional performance with delay as encountered with the power conservation aspects. Furthermore, the Examiner has relied upon the teachings of Li to teach and suggest user specified performance constraints. The Examiner identifies sections 4.3 and 5.2 of Li to evidence a combination of goals or objectives. For example, goal three (III) is to find a set of solutions within performance and energy constraints and this will provide important trade-off information to the designer. Furthermore, section 5.2 of Li and Table 1 teaches and suggests the objectives are energy dissipation and execution time (number of clock cycles). Li further teaches the use of a

minimum energy dissipation while not exceeding the budget of clock cycles to execute. The Examiner relies upon this budget of clock cycles to further evidence that the user would have specified what the budget of clock cycles would be. (Ans. 21). We agree with the Examiner's interpretation. Hence, we find that both Bartley and Li teach and fairly suggest a balancing between power dissipation and performance constraints. While each reference has a different end use and therefore different priority, the two references clearly teach a balance between power dissipation and performance constraints, set forth by a user/designer.

Appellants further contend that Li has nothing to do with inserting power down instructions in code. Appellants further contend that the teachings of Li are very inflexible and are directed to embedded and dedicated hardware platforms wherein once optimized it is done. Thus, Li teaches away from the ability or even any desire to use power control instructions and programs. (App. Br. 11). We disagree with Appellants' limited interpretation of the teachings and suggestions of Li and find that Li teaches and fairly suggests a balancing between power consumption and system performance constraints. When taken in combination with the power down instructions as taught by Bartley, the suggestion of Li would have fairly suggested a balancing of the trade-offs between power dissipation and user specified performance constraints.

Appellants further contend that the system of Li is "very different from the power down aspects of the present application and Bartley" and there is "no consideration of powering down different components." (App. Br. 11). We find Appellants' argument is not commensurate in scope with the express language of independent claim 1 wherein the claim language

does not expressly recite powering down different components. Therefore, Appellants' argument is not persuasive of error in the Examiner's initial showing of obviousness.

Appellants argue at length that the combination of Bartley and Li would be unlikely and that great differences in architecture and methodology "places the likelihood of success of such a combination in great jeopardy." (App. Br. 12). Appellants further contend that the Final Office action fails to explain the relationship between the determination of a threshold relating to a duration of a program segment for a related functional unit, and the insertion of power down instructions that satisfy user-specified real-time performance constraints. (App. Br. 12-13). We disagree with Appellants' conclusion and find that the Examiner's further explanation of the teachings of each reference and the line of reasoning used in the combination to be reasonable in light of the broad language recited in independent claim 1. (Ans. 18-26).

Appellants further argue in the Reply Brief that the Examiner has not shown that Bartley and Li are properly combinable. (Reply Br. 3). Throughout the Reply Brief, Appellants maintains that Bartley and Li are not properly combinable. Appellants further maintained that the claimed invention allows one to determine where among many places in the code that one can add a power down instruction to "optimize power consumption within the user-specified constraints." (Reply Br. 4). Appellants maintain that Bartley relates only to specific locations in the code to place power down instructions to turn off functional units that are not being used, but the presently claimed invention on the other hand relates to a plurality of places in the code, not just places at which functional units are invoked, to placed

power down instructions based on user-specified constraints. (Reply Br. 4). We find each of these arguments are based upon limitations which are not expressly found in the language of independent claim 1. Independent claim 1 neither sets forth "optimizing" power consumption nor specifies "specific locations" for power down instructions. Therefore, Appellants' arguments which are not commensurate in scope with the express language of independent claim 1 do not show error in the Examiner's rejection based upon obviousness.

Appellants further argue that modifying the software in connection with designing memory as disclosed in Li has "little relation" to inserting power down instructions to power down functional units as in Bartley, and hence one of skill in the art at the time the invention was made would not have been led to combine Bartley and Li. (Reply Br. 5). We find Appellants' argument with respect to "little relation" to not show error in the Examiner's proffered combination of teachings. Therefore, we find Appellants' arguments relating to the combination of the teachings to be unpersuasive of error in the Examiner's initial showing of obviousness. Hence, Appellants have not shown error in the Examiner's initial showing of obviousness, and we will sustain the rejection of independent claim 1 and independent claims 14, 24, and 34 and their respective dependent claims grouped therewith by Appellants.

With respect to dependent claim 3, Appellants rely upon the same arguments advanced with respect to independent claim 1. (Reply Br. 13). Since we did not find Appellants' arguments persuasive with respect to independent claim 1, we similarly do not find the same arguments

persuasive with respect to dependent claim 3 and dependent claims 4 -10, 16-21, 26-31, and 37-42 grouped therewith by Appellants.

With respect to dependent claim 11, Appellants argue that the teachings of Li do not deal with power down instructions and therefore cannot disclose the limitation of "a number of power down instructions that can be inserted in an execution path, including one or more identified potential locations." (App. Br. 14 and Reply Br. 5). We agree with Appellants, but find that the Examiner identifies in the Answer at pages 27-28 that it is the combination of teachings with the "budget" that the programmer/user must specify for the execution time constraint in combination with the location for power down instructions. We agree with the Examiner's proffered combination of teachings and find that with the suggestion of specifying constraints, it would have been readily apparent to those skilled in the art that the number of power down instructions that can be inserted in an execution path and specified potential locations would have been desirable as user-specified constraints. Therefore, we find Appellants' argument unpersuasive error in the Examiner's initial showing of obviousness, and we will sustain the rejection of dependent claim 11 and dependent claims 12, 22, 32, and 43 grouped therewith by Appellants.

V. CONCLUSION

For the aforementioned reasons, the Appellants have not shown that the Examiner erred in the rejection based upon obviousness. Furthermore, Appellants have not shown that the prior art references of Bartley and Li do not teach or suggest satisfying user-specified real time performance constraints on the microprocessor as recited in independent claim 1 and

Appellants have not shown that the teachings of Bartley and Li are not properly combinable.

VI. ORDER

We affirm the obviousness rejections of claims 1-44.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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